

# Protection techniques ensure µC reliability in power-control circuits

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Protecting the µC is critical in power-control applications. Protection methods range from limiting input voltages and noise spikes to preventing an out-of-control program from locking up the µC.

Countless numbers of products contain microcontrollers (µCs) that manage critical control elements. In large motor-control systems, failure of the µC or other critical components to perform properly can cause serious injury to the users or bystanders. You need to take special steps to protect the µC in such systems. Because the µC manages most, if not all, of the control design's functions, understanding how to properly protect the µC will lead to more reliable controls. By incorporating numerous protection methods, you can greatly improve the reliability of the µC.

Adequate protection comes in many forms. Various methods that limit voltage spikes—such as simple RC filters and voltage clamps—greatly increase the µC's reliability in power-laden designs. Depending on the application and EMI concerns, simple RC filters do not exhibit the abrupt voltage response of diodes or zener clamping devices. Setting the frequency response of each µC line using filter networks minimizes unwanted noise spikes from corrupting valid signals. In addition to controlling voltage levels, noise spikes and EMI, you need to deal with potential program bugs and environmental concerns.

## Now the failure modes

Fortunately, designing a reliable fault-tolerant µC-based product is not too difficult when you recognize the areas of inadequate protection. Figure 1a shows a typical power-con-

trol circuit and the problem areas; the circuit in Figure 1b incorporates various protection circuits to prevent those problems. Several potential failure modes can occur, including the following:

- Intermittent power or sensor connection (loose wires or connectors),
- Reversal of power connections (user hookup error),
- Power-stage transistor short (induced by poor thermal interface or short),
- µC computational error (caused by undiscovered software bug),
- Latent ESD damage to active components (static charge during assembly),
- Motor-bearing failure (poor lubrication or excessive revolutions per minute),
- Motor-shaft lockup due to external mechanical mishap (user misuse),
- A few more that you can't imagine but will happen (unknown failure modes).

"Unknown failure modes" is the most disconcerting category. You need to understand which part of the electronics system is the most potentially dangerous and then decide how to deal with it. In the motor-control example of Figure 1, the motor is the most hazardous element. In the case of an open sensor or software glitch, turning off the power stage, which turns off the motor, is appropriate. This action disables the motor, thereby stopping any mechanical movement that may cause harm. Such thinking is a good start but assumes that the power stage or the µC control device is not one of the parts that can fail.

In addition to motor controllers, other µC-based designs that control ac loads or relays are also more prone to damage than, for instance, a µC in office computer equipment. Office computers typically use well-regulated power supplies, usually operate in a mild operating environment, and have probably been subjected to EMI design rules. A µC that drives a relay directly or indirectly is subject to voltage tran-

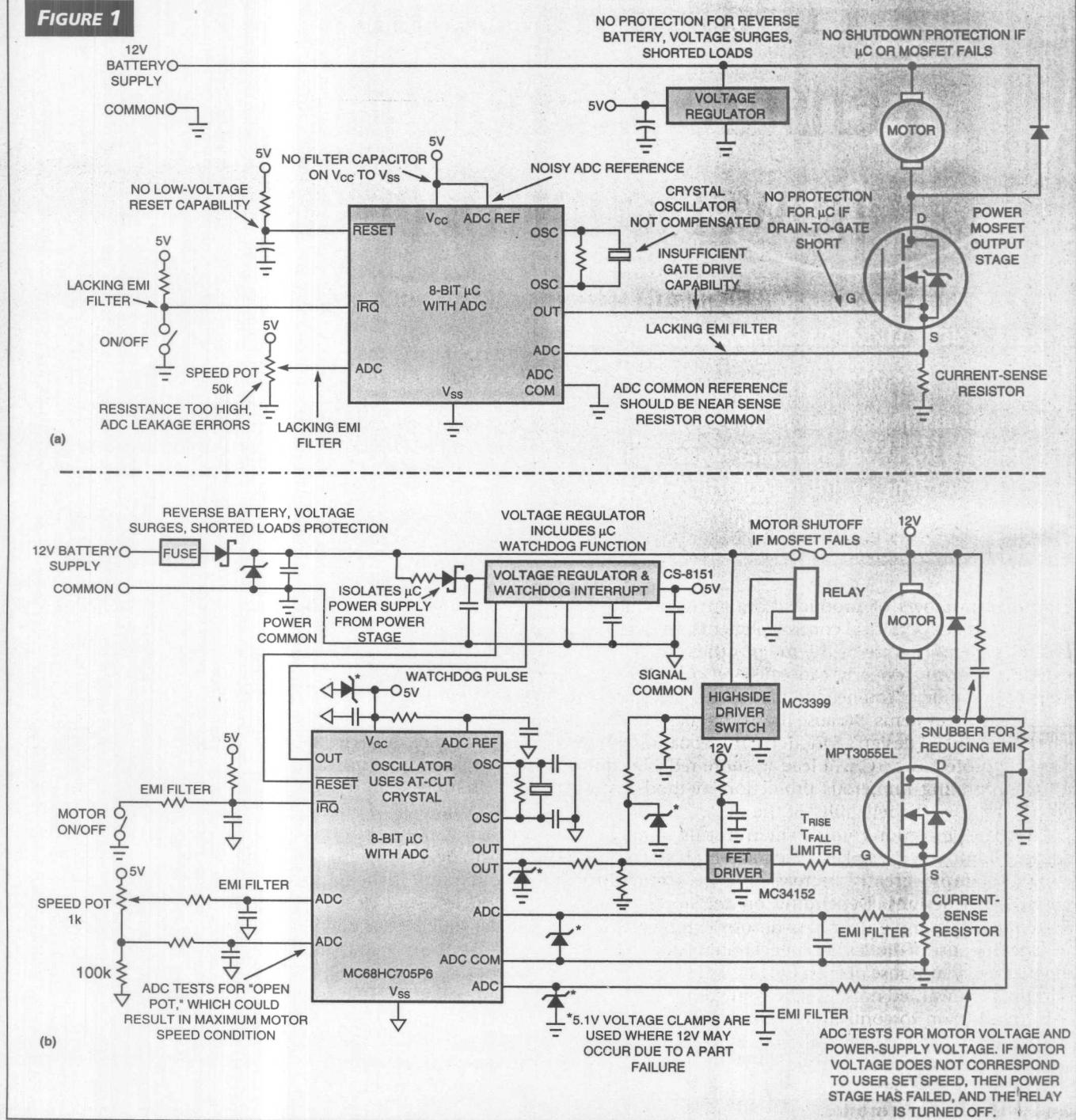
## PROTECTING $\mu$ Cs IN POWER CIRCUITS

sients that the relay's inductive coil causes and to RF noise that arcing across the contacts of the relay generates.

Even seemingly innocuous designs, such as driving an indicator lamp or LED, can cause problems. For instance,

problems can occur if you install the lamp or LED where a person can touch them and induce sufficient ESD into the connecting wires that lead back to the  $\mu$ C. Also, battery-powered  $\mu$ C equipment is susceptible to several problems:

**FIGURE 1**



A  $\mu$ C power-control circuit can contain many potential problem areas (a), but you can use numerous protection methods to eliminate these problems (b).

ESD from the user, EMI from nearby high-powered electrical/electronic equipment, reverse battery hookups, and extreme temperature/humidity environments.

In addition to system-related problems,  $\mu$ Cs are susceptible to their own particular problems. Excessive voltage levels are exceptionally dangerous to semiconductors. Exceeding the semiconductor's breakdown-voltage threshold can burn a hole into the transistor's die in a few microseconds depending on the voltage spike's energy level. The exact failure effect correlates to the voltage fields and current densities in the semiconductor's structure. The typical  $\mu$ C data sheet for an MC68HC05 (or similar device), for example, lists maximum voltage and current levels that the  $\mu$ C can survive. An interesting aspect of these maximum ratings is that the  $\mu$ C can still succumb to an operational failure but not suffer permanent electrical damage when subjected to voltage or current levels that are within its maximum data sheet's specifications.

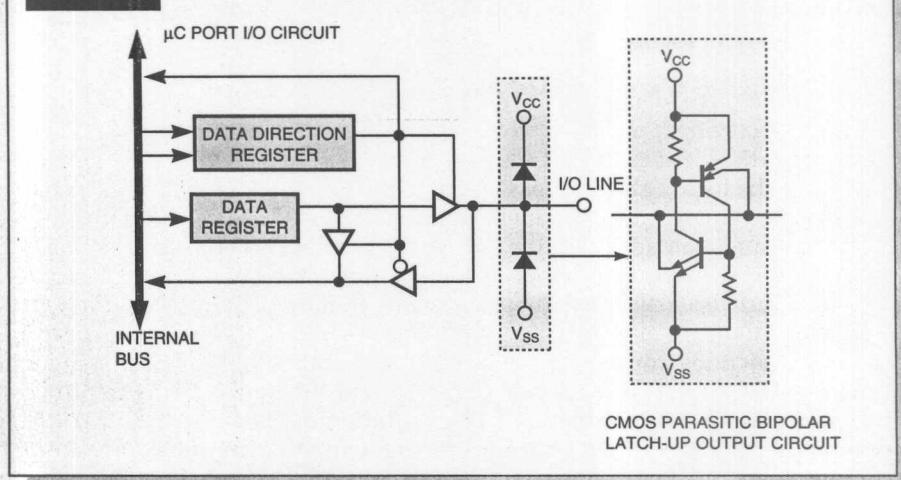
Figure 2 illustrates a typical  $\mu$ C's I/O-port circuit design. Internal diodes connect from the port line to both supply voltage ( $V_{CC}$ ) and common ( $V_{SS}$ ). These diodes conduct and clamp the input voltage if the port-line voltage level exceeds  $V_{CC}$  by about 0.5V or exceeds  $V_{SS}$  by about -0.5V.

Relying on the internal diodes to contain excessive voltage transients on the  $\mu$ C I/O lines is not recommended, especially if the clamp current levels are above a few microamps. When internal diodes operate as clamps, current has to flow through micron-sized pathways or metalization in the  $\mu$ C and out to the common or  $V_{CC}$  bus. If several port lines are in a clamp mode, the total clamp current can reach levels that create significant voltage drops in the internal  $V_{CC}$  or  $V_{SS}$  pathways. These voltage drops can affect the  $\mu$ C logic states or, even worse, can generate enough heat to cause permanent damage to the  $\mu$ C's structure.

Using the  $\mu$ C port lines to conduct clamp current can also lead to more trouble than just excessive power or voltage drops if the external voltage transients contain high frequencies. As Figure 2 shows, the  $\mu$ C internal clamp diodes are likely to be more complex bipolar elements that are subject to latch-up under certain conditions. These conditions include voltage transients of an RF nature that many wireless types of applications can generate.

Externally generated noise spikes on any  $\mu$ C line can induce erratic operation. These spikes can cause the program to crash or lock up, can cause data-direction registers to change state, and can reset or corrupt internal timers. Noise spikes are a normal design consideration in any  $\mu$ C design. As a quick test, EMI experts recommend that you operate a high-powered cellular or mobile transceiver in close prox-

FIGURE 2



**The simple diode clamps on the I/O lines may in reality be more complex structures that can cause latch-up problems if subjected to signals with extremely fast slew rates.**

imity to the  $\mu$ C prototype design. If the  $\mu$ C locks up or operates erratically, serious EMI lab testing is in order. Operating the  $\mu$ C prototype design near an automotive-ignition system gives a good indication of EMI tolerance. ESD test generators are also available that can apply ESD to the external wiring, switches, and control panel to verify ESD endurance.

#### Protect against an out-of-control program

You must also guard against an out-of-control program. Some op-codes exist that can invoke some  $\mu$ Cs into a self-test mode. If, by chance, an out-of-control program or a "hole" in the program manages to allow the  $\mu$ C's program register to load and execute a special self-test code, the  $\mu$ C ignores its user program and performs a built-in self-test routine. Usually, only a complete power-down and normal start-up can reset the  $\mu$ C out of a self-test mode. Some programmers actually search all of their assembly object listings for any of these self-test data codes and rewrite the program to eliminate these particular codes. Raising a certain pin to an abnormal voltage level during a reset can also invoke unwanted self-test modes.

Check with the  $\mu$ C manufacturer to verify how the self-test mode operates and then take steps to ensure that your system doesn't inadvertently invoke this mode during the application's normal operation. You can write some initialization routines to perform a limited circuit test of the application. If this test detects a failure, you can put the controller in a "service required" mode. Testing both critical input-sensor lines and power-stage control lines is recommended practice. Some applications dedicate a  $\mu$ C to perform just this function at all times.

A technique to catch an out-of-control program is to add several "no-ops" instructions followed by a software interrupt at the end of each program sequence or subroutine.

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(The software interrupt halts other program activity, and you use it instead of a jump instruction.) The software-interrupt routine forces a reset of the  $\mu$ C and can toggle an I/O line to alert the user or programmer that a major program error has occurred. Another method to help ensure reliable  $\mu$ C operation is to use two identical  $\mu$ Cs whose output lines are fed to an AND gate. Both  $\mu$ Cs have to compute the same results and output the identical logic 1 signals before the AND gate will allow the logic 1 signal to pass through to a power-control stage or other critical output element.

The normal watchdog routine, in which the program must periodically reset an internal or external timer, can also detect a program lockup. The no-op instructions followed by a software interrupt may detect a program fault faster than can the watchdog routine, depending on the watchdog timer's value. Other items that cause mysterious program faults are a poor reset-control circuit, floating interrupt lines, or power-supply brownouts. Often, the program runs fine in the development-system environment but fails after you electrically program the  $\mu$ C and run it in a stand-alone mode. In many cases, this failure results from an incorrect reset or interrupt design in the user's circuit. The development system usually has some type of built-in reset and interrupt-control circuits that allow the  $\mu$ C to operate.

You should terminate all unused  $\mu$ C pins with pullup or pulldown resistors. Directly connecting unused lines to  $V_{SS}$  or  $V_{CC}$  can spell trouble if the  $\mu$ C inadvertently sets the port line's data-direction registers as outputs, which might happen with an out-of-control program or simple program error.

Another reason to use termination resistors rather than direct connections is that, during reset, all of the  $\mu$ C port lines go to a high impedance, allowing output lines to float. This high impedance can wreak havoc if the output lines are directly driving a high-impedance power device, such as a power MOSFET. Any slight leakage or EMI can turn on the MOSFET during the reset period, which lasts until the  $\mu$ C

starts executing the port-initialization code. Note that some  $\mu$ Cs include internal I/O-port-termination resistors to minimize this problem.

### Understand the basis of EMI problems

Dealing with EMI problems is a large part of ensuring a reliable product. Realizing what causes EMI requires a review of some fundamentals. Familiarity with the limitations of various CAD tools and  $\mu$ C-development systems is also important.

You normally control an inductive load using a device, such as a relay/contactor or power transistor, to switch the current through the inductor. A  $\mu$ C output-port line can also directly control low-power loads. The difficult aspect of switching inductive loads is that, when an inductive load is switched off, a collapsing magnetic field builds up a counter voltage (CEMF) whose amplitude is related to the inductance, coil current, coil resistance, and the rate at which the current switches off. The formula to calculate the inductive kickback voltage is

$$E_{PEAK} = L(di/dt),$$

where  $E_{PEAK}$  is the kickback voltage,  $L$  is the inductance in henries,  $di$  is the current amplitude delta in amperes, and  $dt$  is the time period of the switching event in seconds.

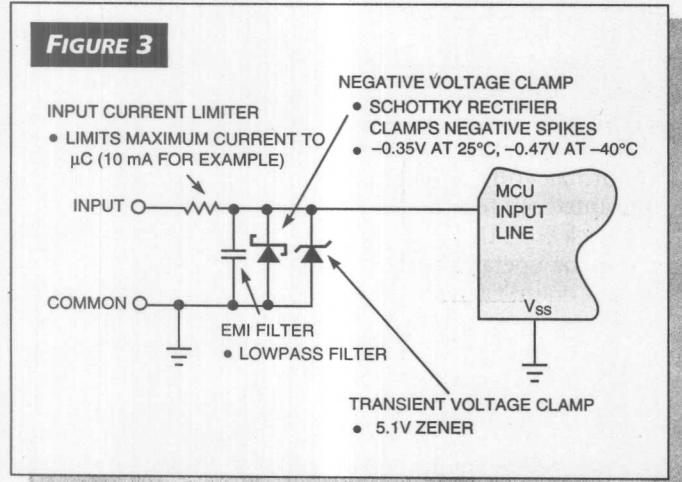
Putting this formula into practice reveals that the fast  $\mu$ C switching speeds—typically 50 nsec—and miniature 5V relays or any inductive load can generate a significant kickback voltage. Miniature 5V relays typically have coil inductances of tens of millihenries. Generally, lower coil currents mean more windings, which results in higher inductance values. A test of three generic 5V miniature relays indicated the following coil resistance and inductance values: 55Ω with 26 mH, 70Ω with 65 mH, and 250Ω with 77 mH. Using the previous formula, theoretical peak voltages of over 20,000V are possible if these miniature relays switch at 50-nsec speeds. Adding a simple clamp diode across the coil is the usual fix, but introduces another set of problems.

When you initially energize the relay coil, its current rises at a slope mostly controlled by the coil's inductance and resistance values and by the applied voltage. The inductor's current continues to ramp up, with the dc resistance generally limiting the maximum level. If the coil's pulse width is too narrow, the coil current may not reach its maximum value, which reduces the kickback voltage. This lower voltage may not correctly operate the relay mechanism.

You should keep track of the maximum inductance values of any component that electronic devices switch. This statement holds true for so-called "noninductive" devices, such as lamps or resistors. All components have a certain amount of inductance, which will become critical when the switching edges are too fast.

When an open-collector (bipolar type) or open-drain (MOSFET type)  $\mu$ C output line switches any inductor, the inductor's kickback voltage can easily exceed the transistor's breakdown-voltage rating and may cause a secondary-breakdown failure. Once the transistor enters secondary break-

**FIGURE 3**



**Input-line protection methods include a series resistor for current limiting, voltage clamping, and the suggested ubiquitous RC filter.**

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down, its blocking voltage diminishes, and the remaining inductive energy literally burns a hole into the silicon chip. Some power transistors, such as avalanche-rated power MOSFETs, act like zener diodes if the blocking voltage exceeds nominal. These transistors do not fail until their power-dissipation rating exceeds the maximum.

### PC-board layout affects EMI

Most designers use software layout tools to design pc boards, and several such programs use an autorouter to connect the traces. This method works fine for low-speed and low-current circuits. However, big problems usually occur when an autorouter places high-speed and high-current lines without some guidance from an EMI-knowledgeable engineer. Some companies actually require that experienced EMI engineers operate the layout tools.

A few general rules can help minimize EMI difficulties in pc-board layouts:

- Make high-current switching lines as short and as wide as possible.
- Use the "three-to-one" layout rule: the trace width should not be less than one-third of its length.
- Route clock lines or high-speed lines near  $V_{CC}$  or  $V_{SS}$ .
- Slow switching edges if possible.
- Carefully route ADC lines; don't mix the reference pins with the  $V_{CC}$  and  $V_{SS}$  current-carrying traces.
- Follow the pc-board-layout rules that the  $\mu$ C data sheet or application note recommends.

When analyzing EMI problems, remember the basics: the maximum frequency and amplitude of the generated or received signal; the time and place that the EMI occurs (such as, failures occur every time a high-power radar antenna swings into sight or when the circuit is near high-voltage power-distribution lines); the impedance of the suspicious network; and the physical aspects of the traces or wiring.

Clock and oscillator circuits can be potential EMI problems. Most  $\mu$ C manufacturers usually recommend a particular oscillator pc-board layout. Recent  $\mu$ Cs use low-power oscillator designs to minimize radiated emissions. Placing a small metal shield around the entire  $\mu$ C and associated components can also be effective to minimize EMI problems.

Be sure to adequately decouple the  $V_{CC}$  line, because this line conducts high-frequency currents. The placement and values of the  $\mu$ C's  $V_{CC}$  decoupling capacitors are somewhat critical. The capacitors should be close to the  $V_{CC}$  and  $V_{SS}$  pins.

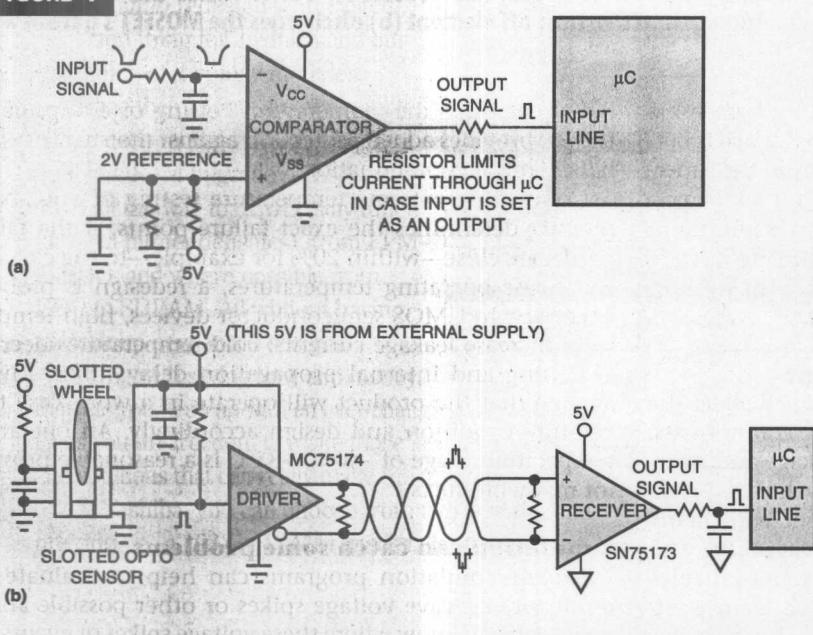
### Program bugs can bite

An external voltage spike that upsets the  $\mu$ C's internal logic can cause an out-of-control program. Undetected errors in the program can also cause a failure. Programs in  $\mu$ Cs tend to be hand-packed to minimize ROM size and increase throughput. Unfortunately, errors can creep in. Even programs written in high-level languages can fail if there is a bug in the compiler, for instance.

Most  $\mu$ C-control designs deal with external events and generally use timers as part of some calculation. When a timer generates an interrupt or an external event needs servicing, the normal program flow halts, and the  $\mu$ C processes the interrupt. Because external events can interrupt the user's program at any time and thus can halt the main routine or its subroutines (depending on preset control logic), these routines can get lost during one of these numerous interruptions. This problem can happen if too many subroutines are nested together, allowing the program stack RAM to read/write into normal user RAM.

If a random glitch does occur during the course of debugging a  $\mu$ C program or testing the  $\mu$ C system, you should not dismiss the problem without recording the conditions that were present. If another random glitch occurs again, you can compare it to the first to determine if the events that caused the glitch are truly random. The  $\mu$ C-development tools can help if they are capable of real-time analysis. Most low-cost  $\mu$ C-development systems are adequate for preliminary program development but lack the sophistication to show exactly what is happening inside the

FIGURE 4



**A buffer comparator (a) can convert a slow slew-rate signal into a pulse suitable for triggering a timer input. A twisted-wire-pair driver and receiver (b) is useful in a noisy application, such as a motor-speed sensor.**

$\mu$ C's CPU and control registers during reset, interrupts, and timer rollovers.

### Watch for a sagging $V_{CC}$

Some  $\mu$ Cs may not recover well if the  $V_{CC}$  sags momentarily. This situation is different from a normal power-down/power-up condition when the  $V_{CC}$  drops to zero and then goes back to its normal value. The  $\mu$ C's internal power-on reset usually can deal with a normal voltage swing from zero to full  $V_{CC}$ . However, if  $V_{CC}$  slowly sags by 50% and then slowly rises to normal, the  $\mu$ C may not recover. External  $\mu$ C-supervisory devices, such as the MC34160, MC34164 (both from Motorola, Tempe, AZ), MAX814 (Maxim Integrated Products, Sunnyvale, CA), and CS-8151 (Cherry Semiconductor, East Greenwich, RI), can monitor the  $V_{CC}$  bus and generate a reset when  $V_{CC}$  sags.

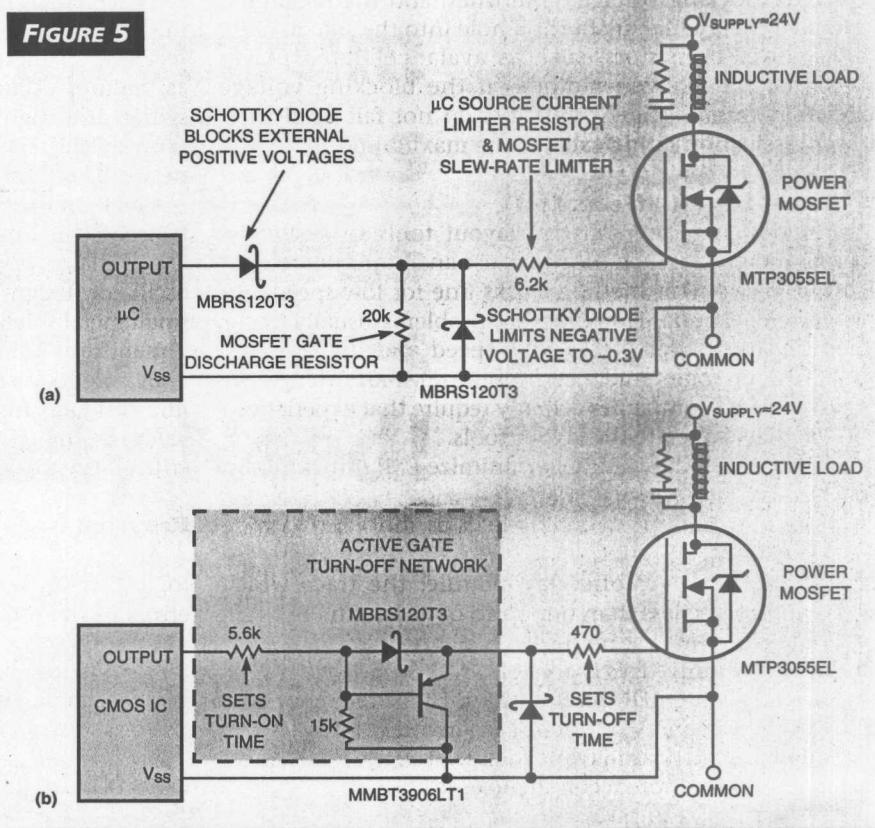
A good test to determine whether the  $\mu$ C is vulnerable to brownout is to run the  $\mu$ C at normal voltage, slowly decrease the  $V_{CC}$  until  $\mu$ C errors occur, and then raise the  $V_{CC}$  slowly back to normal. If the program does not recover, a power-supply-supervisory design is necessary. Supervisory devices are frequently worth the extra cost in  $\mu$ C power-control designs, and you should design these devices in from the beginning. If rigorous testing shows the supervisory circuit is not necessary, simply don't assemble the parts onto the pc board. Some small wasted space is better than having to redesign the board later to add the supervisory circuit. If you use a low-voltage detection and supervisory device, its operation should match the  $\mu$ C's minimum  $V_{CC}$  specifications. For example, if the  $\mu$ C is rated to operate at  $5V \pm 10\%$ , the supervisory device should force the  $\mu$ C into a reset mode if the  $V_{CC}$  sags below 4.5V.

### Account for the operating environment

Temperature, thermal shocks, and moisture all affect the long-term reliability of most active electronic components, including  $\mu$ Cs. To a high degree, the  $\mu$ C package and internal die-mounting methods determine how well the  $\mu$ C will hold up long-term in a stressful environment with many power-control systems. A low-cost plastic package may suffice for applications in an office environment, but for automotive under-the-hood or motor controls in a factory setting, superior  $\mu$ C packages are necessary.

Some design methods can also increase the  $\mu$ C's chances of survival in a hostile environment. Using the lowest clock frequency possible keeps the  $\mu$ C's power dissipation low. Using a heat sink or other cooling device on the  $\mu$ C helps to

FIGURE 5



This circuit (a) provides output-line protection but switches the MOSFET rather slowly. Adding an active turn-off element (b) discharges the MOSFET's gate at a fast rate.

reduce the  $\mu$ C's die temperature. Potting or encapsulating the  $\mu$ C provides added protection against moisture or external chemical contamination.

Conducting extreme temperature testing of a  $\mu$ C-based product determines the exact failure points. If the failure points are close—within 20% for example—to the expected worst-case operating temperatures, a redesign is probably necessary. In CMOS semiconductor devices, high temperatures increase leakage currents; cold temperatures decrease switching and internal propagation delay times. Always assume that the product will operate in a worst-case temperature condition and design accordingly. An operating temperature range of -40 to +85°C is a reasonable prospect for many products.

### Simulation can catch some problems

Circuit-simulation programs can help to evaluate the results of excessive voltage spikes or other possible abnormalities if you know where these voltage spikes or events will occur. The simulation program's accuracy is limited by the model's specifications and, in general, you can't totally trust such programs to find all the potential problem areas. Many semiconductor models are not 100% complete or up-to-date.

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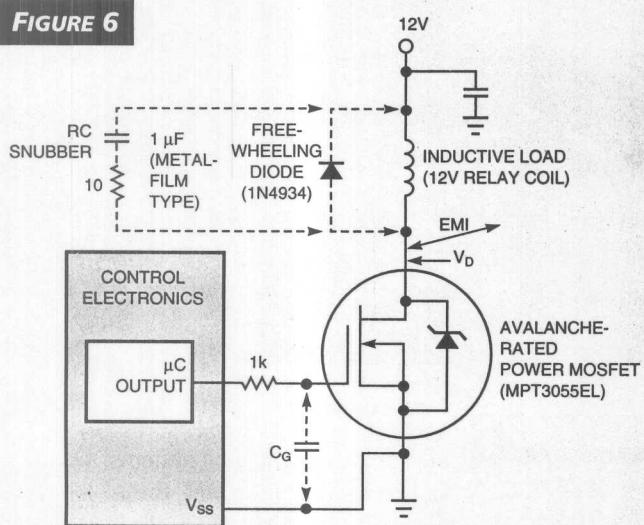
and may not have been thoroughly tested in unusual modes of operation.

Thus, simulation programs are powerful tools for developing circuits and even system-level designs, but they cannot guarantee that the actual product is totally perfect. In some cases, the simulation results that do show problem areas are not immediately obvious. Generally, trouble spots occur on or near signal transitions. You should examine these areas on at least a 1- $\mu$ sec scale with a minimum simulation resolution of 10 nsec.

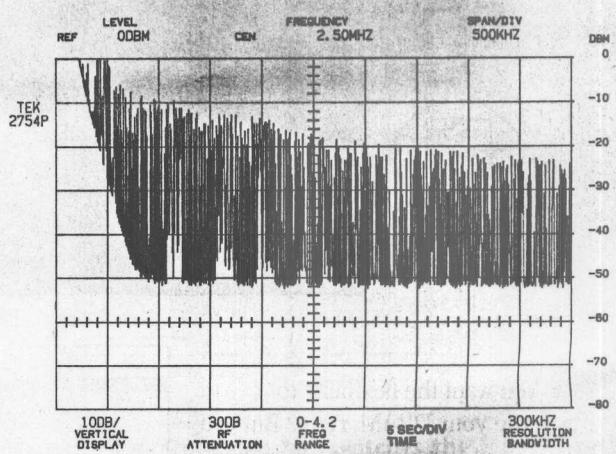
Because simulation can't reveal all problems, hardware

debugging is inevitable. Unfortunately, digital oscilloscopes can hide or filter out fast, narrow voltage spikes. Always search for voltage spikes with a timebase setting that can reliably show 10- to 50-nsec signals. Using a slow 100- $\mu$ sec timebase often does not show the trouble spots. Using an analog oscilloscope to catch a fast single event mixed in with a lower frequency repetitive signal isn't easy. Digital scopes are very good at capturing fast single-event signals, provided that you properly set the scope. You can miss fast nonrepetitive pulses when the digital scope is set to display a much slower repetitive-type signal. You may have to use different types

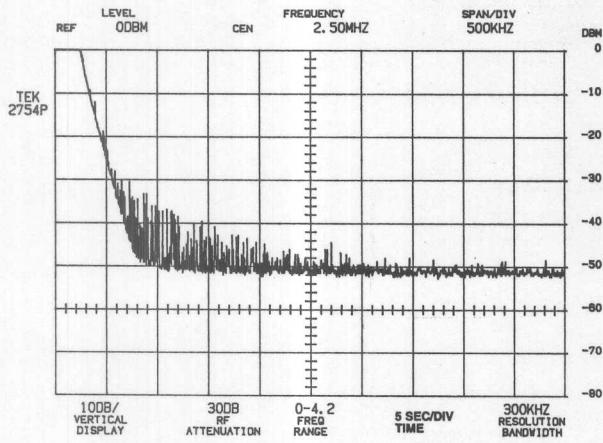
**FIGURE 6**



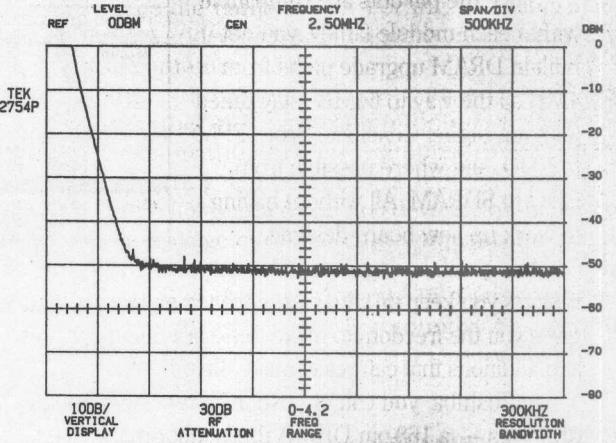
(a)



(b)



(c)



(d)

A simple switching circuit (a) can produce high levels of EMI (b). Adding a freewheeling diode removes the voltage spike at  $V_D$ , but does not decrease EMI levels. Adding a 0.1- $\mu$ F capacitor,  $C_s$ , does significantly reduce EMI (c). Finally, using  $C_s$  and replacing the freewheeling diode with an RC snubber produce the lowest EMI results (d).

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of oscilloscope to look for different signals. Three types of oscilloscopes good for debugging  $\mu$ C-control designs are a 120-MHz analog storage scope; a general-purpose, 150-MHz digital scope; and a 2-GHz digital scope. You can also use a spectrum analyzer for EMI testing.

### Consider the circuit-design solutions

Fortunately, you can protect your circuit against potential overvoltage, EMI, low-voltage, program, and environmental problems. Design methods that can minimize these problems start with a basic principle: use lowpass filters on every  $\mu$ C line to set the upper frequency limit, depending on the application. Without these filters, the  $\mu$ C lines act as antennas, and the  $\mu$ C's internal logic circuits and program stability suffer.

Voltage spikes from noninductive sources can couple by parasitic capacitance into the  $\mu$ C lines by various means: poor pc-board layouts, insufficient isolation between  $\mu$ C lines to the power-control stage, or mounting the  $\mu$ C too close to a high-voltage field source. One starting point in protecting the  $\mu$ C-input lines would be to assume that all  $\mu$ C lines can be exposed to voltage spikes similar in magnitude to the worst-case voltage levels in the system. For example,

in an automotive application, any line

that leads to the outside can be exposed

either vehicle ground or full battery

voltage. In a motor-control applica-

tion, the  $\mu$ C external lines may be sub-

ject to full ac-line voltages.

Magnetic coupling can also be a problem if the  $\mu$ C's lines or the  $\mu$ C itself is located near an intense magnetic-field source, such as a high-power transformer or high current power conductors. You can use metal shields to reduce magnetic coupling.

Figure 3 shows protection methods for  $\mu$ C-input lines. The basic method is to use zener or Schottky diodes for voltage clamping and series resistors for current limiting. You should also include the capacitor to form the RC filter. These methods work well for  $\mu$ C-input lines. Set the RC filter's time constant for the lowest frequency possible.

Input ports, such as timer inputs, are sometimes set to toggle on switching edges and require a minimum dv/dt to operate correctly. For this type of input, the RC-filter method may not suffice, and a buffer element may be necessary (Figure 4a). The buffer consists of a comparator with high gain, and a trip

int is set approximately midway between  $V_{CC}$  and  $V_{SS}$ . You can modify the comparator design to allow hysteresis, which has the effect of a Schmitt trigger; the circuit converts an

input signal, such as a sine wave, with slow rise and fall times plus some noise into a pulse with fast switching edges.

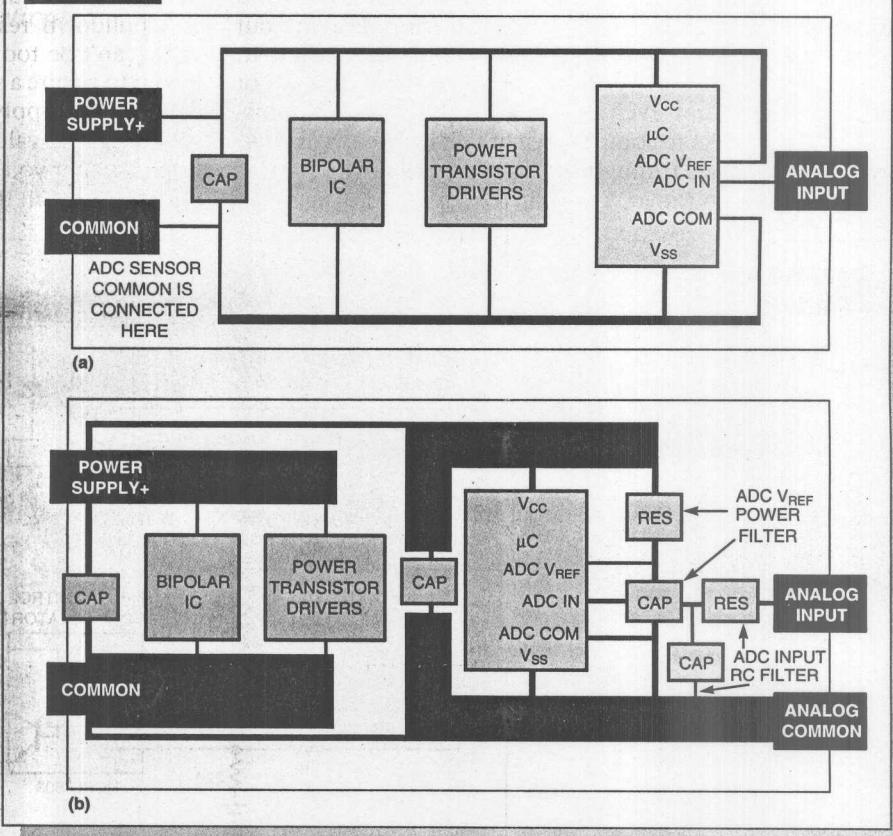
### Buffer serial-data lines

For serial-data lines that must work in an electrically noisy environment, you can also use a twisted-wire-pair transceiver to clean up noisy input signals (Figure 4b). This receiver design has high common-mode noise rejection and a low impedance. The differential line drivers and receivers operate from -7 to +12V common mode, making this design suitable for many electrically noisy environments, such as a motor-speed and angular-position sensor.

In Figure 4b, the speed-sensor transmitter circuit uses a slotted optical switch, a high-performance line-driver IC, and a TO-220-sized 5V regulator. The slotted optodetector uses Schmitt-trigger logic, which provides hysteresis for noise immunity and pulse shaping. The twisted-wire pair connects to the receiving circuit that uses a quad differential line-receiver IC. The receivers connect to the motor drive's  $\mu$ C-input port. A simple lowpass RC filter slightly slows the speed sensor's signal, which helps to clean up the signal in the presence of strong RF fields.

In addition to input lines, you should also pay particular

FIGURE 7



A poor pc-board layout uses narrow traces for power and ground, and allows the power traces to mix at various points on the board. An improved version (b) splits the power traces back to their source points.

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attention to interrupt and reset lines to minimize the chances of extraneous voltage spikes. You can program some  $\mu$ Cs to respond to either edge-triggered or level-sensitive external interrupts. Using the level-sensitive option allows more noise immunity at the expense of reduced response time to an external event that forces an interrupt.

To check some of these input connections, you can program the  $\mu$ C to perform some simple debugging steps. (You can also use a real-time development system if available.) One debugging method to verify that an external event or any particular routine is functioning correctly is to toggle an unused output port when a particular event happens. For example, if an external pulse is supposed to drive an internal  $\mu$ C counter whose value is used to perform some calculation, you want to know that the input pulse increments the counter only once. A noisy input pulse may advance the timer incorrectly. If an output pulse occurs every time the  $\mu$ C increments its counter, an external oscilloscope can verify the operation. You may also discover that both an errant program routine and a poor pulse input are toggling the timer.

### General output-line considerations

As previously discussed, connecting a  $\mu$ C directly to an inductive load usually requires voltage-clamping networks to protect the  $\mu$ C's internal silicon structures. Leaving out some form of voltage-transient protection may result in minor erratic program operation or, in the worst case,  $\mu$ C or other device failures. Even an  $\mu$ C indirectly driving an inductive load is subject to some degree of voltage-transient energy that propagates through the load-control power transistor and back into the  $\mu$ C's output-port line.

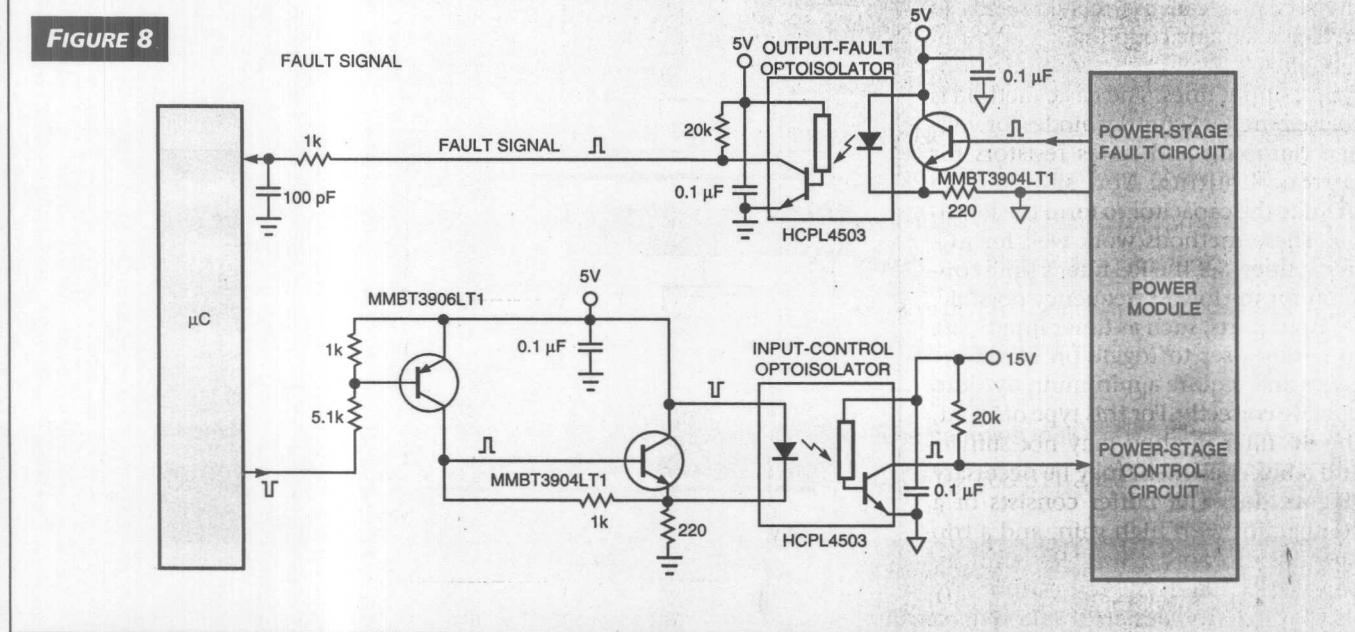
Sometimes, the power device fails first because of its inadequate protection against excessive CEMF or other load faults. If the power-device design does not limit the actuator's CEMF voltage or protect against power-supply voltage spikes, the power device may self-destruct and allow high-energy levels to propagate through the more expensive and difficult-to-replace  $\mu$ C device.

There are several CEMF-protection methods possible. One solution is to select a semiconductor switching device with sufficient voltage-breakdown rating so that it never enters a secondary-breakdown condition. Unfortunately, the word "never" is subject to Murphy's law, and the transistor probably is subject to some degree of overvoltage stress during its lifetime. If the power MOSFET shorts out with a drain-to-gate short (as happens in many cases), the  $\mu$ C-output line is subjected to the MOSFET's full-drain voltage, which could be several hundred volts.

**Figure 5a** illustrates protection for  $\mu$ C-output lines against excessive positive and negative voltage transients. A Schottky barrier diode in series with the output line to the MOSFET provides isolation against positive-going voltages from the MOSFET's drain-to-gate path. This scheme does compromise the circuit's operation by lowering the available gate voltage by one Schottky-diode drop and does not allow the gate to discharge through the  $\mu$ C output.

A pulldown resistor discharges the gate. This resistor's value can't be too low or the  $\mu$ C output gets loaded down too far to ensure a sufficient gate-bias level. A typical 5V-type output can supply 0.8 mA at a level of 4.2V. The corresponding load value is  $5250\Omega$ , which leaves only about 3.9V gate bias after you subtract the Schottky-diode drop. A resistor in series with the gate limits the maximum current from

**FIGURE 8**



Optoisolators provide the proper isolation between the  $\mu$ C and a high-voltage power stage.

## PROTECTING $\mu$ Cs IN POWER CIRCUITS

the MOSFET and establishes a passive element that mostly controls the MOSFET's turn-on switching time. A variation on this method is to add an active turn-off element (Figure 5b).

One additional note about directly driving a MOSFET: The gate-input capacitance can draw a high peak current from the  $\mu$ C. You need to select the value of the series-resistor value to limit the  $\mu$ C peak current to under 10 mA. The MOSFET's turn-on switching time depends on how fast its gate-input capacitance charges up, which may require a significant current peak for a large MOSFET. The  $\mu$ C output thus requires a buffer stage to drive large MOSFETs.

Several MOSFET and insulated-gate bipolar-transistor drivers are available for interfacing the  $\mu$ C output line to drive MOSFETs or similar power devices. There are many other IC devices available for driving lamps, relays, LEDs, or displays that easily interface to the  $\mu$ C.

### Reduce EMI in power control

Figure 6a shows a switching circuit in which a  $\mu$ C drives a simple power-control stage. An avalanche-rated power MOSFET handles the relay's inductive kickback voltage. Unfortunately, this design generates significant EMI that can affect the  $\mu$ C and other nearby sensitive devices (Figure 6b). Two conditions in this switching circuit contribute to EMI: the  $\mu$ C output's high-speed transitions, which drive the power MOSFET, and the inductive kickback voltage, which causes the MOSFET to avalanche (act like a zener diode).

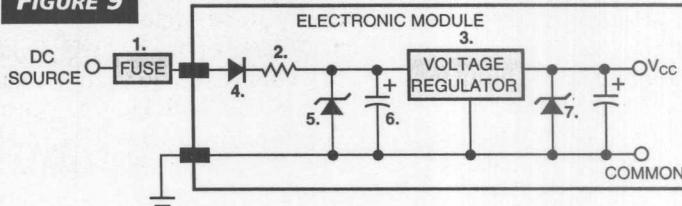
Slowing the switching edges of the  $\mu$ C output that drives the MOSFET's gate helps minimize EMI because the MOSFET's switching times are no longer in the RF range. A  $\mu$ C-output signal can be less than 100 nsec. If the power MOSFET switches at anywhere near this speed, serious EMI will result.

One simple method to slow the signal's edges is to add a series resistor and a gate-to-source capacitor. This scheme is similar to the RC filter for the  $\mu$ C's input lines. To minimize the chance of parasitic RF oscillations during switching, the series resistor value should be 1 k $\Omega$  or less, and the gate-to-source capacitor value should be fairly large—0.01 to 1.0  $\mu$ F—to slow the gate-drive signal-transition times. You should connect the gate-drive source lines close to the source lead and place these lines out of the source lead's load-current path.

Figure 6c shows the positive results of adding a 0.1- $\mu$ F gate capacitor. This RC network is a low-cost fix but does introduce a timing delay and extra power dissipation in the MOSFET. The extra power dissipation occurs because of the power MOSFET's slow turn-off and may require increased heat sinking for the MOSFET.

You should note one other point about using a RC filter in the MOSFET's gate drive. A typical power MOSFET

**FIGURE 9**



1. FUSE PROTECTS AGAINST ELECTRICAL FIRES, BUT GENERALLY DOES NOT PROTECT AGAINST SEMICONDUCTOR FAILURES. THE SEMICONDUCTOR DEVICE USUALLY BLOWS OPEN BEFORE THE FUSE MELTS.
2. A SERIES RESISTOR SETS THE MAXIMUM SOURCE IMPEDANCE OF THE MODULE'S POWER SOURCE. THE RESISTOR WILL LIMIT PEAK CURRENT LEVELS DURING ABNORMAL OPERATION.
3. VOLTAGE REGULATOR ENSURES CONSTANT VOLTAGE TO  $\mu$ C AND OTHER CIRCUITS. SOME VOLTAGE REGULATORS INCLUDE  $\mu$ C RESET FUNCTIONS.
4. ISOLATION RECTIFIER PROTECTS AGAINST REVERSE POWER SOURCE CONNECTIONS—IMPORTANT FOR AUTOMOTIVE APPLICATIONS. SCHOTTKY RECTIFIERS DROP LESS THAN 0.5V.
5. TRANSIENT SUPPRESSOR LIMITS THE MAXIMUM SOURCE VOLTAGE. IT IS VERY IMPORTANT TO PROTECT SEMICONDUCTOR DEVICES FROM OVERVOLTAGES. THE SERIES RESISTOR WILL HELP TO LIMIT THE PEAK CURRENT THAT THE TRANSIENT SUPPRESSOR SUSTAINS DURING A VOLTAGE SPIKE.
6. LARGE FILTER CAPACITOR SMOOTHES OUT VOLTAGE SOURCE FLUCTUATIONS, AND, IF LARGE ENOUGH, CAN HOLD SUPPLY VOLTAGE FOR A FEW SECONDS AFTER MAIN POWER IS SWITCHED OFF. THIS IS USEFUL FOR ENSURING STABLE OPERATION OF MOTION-TYPE APPLICATIONS.
7. OPTIONAL ZENER REGULATOR PROTECTS AGAINST VOLTAGE REGULATOR SHORT AND LIMITS  $V_{CC}$  VOLTAGE SPIKES.

**These power-supply-design elements protect a  $\mu$ C against fluctuating and reversed-power voltages.**

exhibits high transconductance, which means only a small gate-voltage variation is necessary to turn the load on or off. The gate-voltage variation equals the load current divided by the MOSFET's forward transconductance. For example, a MTP3055EL's forward transconductance ( $g_{FS}$ ) is 5.0 mhos minimum. If the load current is 0.2A, then the  $\Delta V_{GS}$  is only 0.04V ( $\Delta V_{GS} = 0.2/5$ ). Therefore, only a small portion of the gate-voltage transition time affects the switching times of the load, and a large gate-to-source capacitor is necessary to slow the gate-voltage transition time. Unfortunately, slowing the power MOSFET may not eliminate EMI, because switching relays or similar type loads with very slow switching is usually not possible.

The other EMI source is from the inductive-kickback voltage. Adding an external diode, which is sometimes called a "freewheeling" diode, across the relay stops the power MOSFET from avalanching and removes a significant spike at  $V_D$ . You might think that this step would significantly reduce EMI. However, the diode's switching is so fast that the EMI is still as high as that in Figure 6b. (Using the freewheeling diode in addition to capacitor  $C_G$  results in EMI levels between those in Figures 6b and 6c.) The freewheeling diode also slows the solenoid's or relay's mechanical turn-off performance.

Replacing the freewheeling diode with an RC snubber reduces EMI and allows a good turn-off mechanical response. The snubber capacitor's value should be large enough to prevent the power MOSFET from avalanching.

The specific application determines the exact value of the RC snubber. However, a 1- $\mu$ F metal-film capacitor and 10 $\Omega$  resistor are good starting values.

Thus, by adding an RC filter to the gate drive to slow the power transistor's switching and an RC snubber across the load to contain the inductive kickback voltage, the  $\mu$ C can drive a power MOSFET with minimal chance for EMI. Figure 6d shows the low EMI that results from using both techniques.

#### Protect the ADC inputs

Reducing errors in  $\mu$ C ADC ports is especially important for applications that constantly monitor the ADC inputs for slight variations. You can trace many ADC errors back to several causes: poor pc-board layout, insufficient filter capacitors, improper placement of the filter capacitors, and a high ADC source impedance.

**Poor pc-board layout:** The most single important design goal is to not mix the ADC grounds and  $V_{CC}$  reference into traces that conduct high pulse currents. Figure 7 illustrates both a poor and good layout for ADC  $\mu$ C signals. Note how the improved version splits the power traces back to their source points.

**Insufficient filter capacitors:** Forgetting that all lines, traces, wires, or internal device leads are always inductive leads to noisy  $V_{CC}$  and commons if you don't use filter capac-

itors of sufficient size and type. In some cases, a separate regulator or power-supply diode isolator is necessary to supply the  $V_{REF+}$  pin of the ADC.

**Improper placement of filter capacitors:** You need to place bypass or decoupling capacitors as close as possible to the source of the high-frequency noise. For a  $\mu$ C design, this means bypass capacitors right at the  $\mu$ C's  $V_{CC}$  and  $V_{SS}$  pins, in addition to the voltage-regulator output and input pins.

**High ADC source impedance:** The  $\mu$ C ADC stage does exhibit a slight leakage current, usually less than 10  $\mu$ A. Thus, to maintain a 1-bit accuracy (0.01953V) for an 8-bit, 5V channel, the total input resistance must not exceed 1.9 k $\Omega$  ( $R_{INPUT} = 0.0195V/10 \mu A$ ). Check the  $\mu$ C's data sheet for the exact ADC leakage current. Adding a simple RC filter to the input is acceptable if the filter's time constant is well below the sample rate required by the application. Remember that you need to keep the RC filter's resistor value plus the voltage source's impedance low to minimize errors.

#### Isolate $\mu$ C lines

Connecting an  $\mu$ C's output or input lines to a high-voltage power stage requires the use of excellent isolation devices. Optoisolators, such as those in Figure 8, provide a high degree of isolation from high-voltage waveforms in large motor drives or power-line-conditioning equipment

(continued on pg 195)

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## PROTECTING $\mu$ Cs IN POWER CIRCUITS

The important specification for any isolation device, besides its maximum isolation voltage, is the common-mode voltage rejection. If there is a large amount of internal capacitance in the optoisolator input-to-output path, the chances are high that enough energy will couple through the optoisolator to cause trouble with a  $\mu$ C line.

To save costs, some designs allow the  $\mu$ C to float on a high-voltage bus. This scheme saves the cost of isolating the  $\mu$ C from the high-voltage bus but requires some form of isolation to the user-operated inputs. The additional difficulty with this method is in field servicing. The technician may accidentally ground out the  $\mu$ C's common with catastrophic results. As a matter of principle, if the  $\mu$ C is accessible for debugging, connecting test probes to it should not represent a lethal hazard for the service personnel.

### Stabilize the power supply

The  $\mu$ C's stability is only as good as its power supply. Power-control circuits can have intermittent power connections or users that play with the power switch. Another common problem is reversed power connections caused by battery reversal or improper hookups. Reversing the  $V_{CC}$  and  $V_{SS}$  on a  $\mu$ C is usually catastrophic to the  $\mu$ C die. Figure 9 shows some simple methods to protect against fluctuating power and reversed power voltages. Adding a zener diode rated just below the maximum  $\mu$ C operating voltage across the  $\mu$ C's  $V_{CC}$  and  $V_{SS}$  pins is good insurance against a shorted regulator or other mishap that would allow excessive  $\mu$ C supply voltage.

A good principle to follow is to physically set the supply's maximum current level. You can use small, surface-mount fuses for this task. In some cases, two different-sized fuses are necessary: one large fuse for the power stage and a small fuse for the control logic.

Adding a series resistor to the power-supply-regulator input also limits the maximum peak-current levels. For example, a  $\mu$ C design that requires only 0.01A from a 12V supply could use a 5V regulator with a 100 $\Omega$ , 2W series resistor in its 12V input side. The 100 $\Omega$  resistor would normally drop 1V but would limit the maximum current to 0.12A in a short-circuit condition. More important, by also adding a zener-diode transient suppressor to the regulator's input, the resistor limits the zener's maximum peak current when the 12V supply is subjected to serious voltage spikes. **EDN**

### Author's biography

**Richard J Valentine** is a member of the technical staff of Motorola Inc's Semiconductor Products Sector (Tempe, AZ). He helps develop semiconductor products for industrial and automotive electronic systems. He holds two patents, has written more than 45 technical articles, and is developing a motor-control handbook.

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